843.37610X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Y. MIYAKI et al.
Serial No.:	09/381,400
Filed:	February 3, 2000
For:	SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD
Art Unit:	2826
Examiner:	A. O. WILLIAMS

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 25, 2003

Sir:

In response to the outstanding non-final Office Action, dated July 25, 2003, the period of response for which extension of time is requested in the attached Petition for Extension of Time, the following discussion and rebuttal arguments are respectfully submitted in connection with the above-identified application.

According to the outstanding non-final Office Action, claims 22-36 stand rejected under 35 USC §103(a) over (1) the newly formulated combination of Kajihara et al (USP 5,637,913) in view of Yamamoto (JP 63-271939) and further in view of Mori (JP 3-22465) and, separately, over (2) the newly formulated combination of Umehara et al (JP 9-97806) in view of Mori (JP 3-22465). (The previously set forth rejection in view of the combined teachings of Kajihara et

al and Yamamoto was rendered moot with the previously submitted response, dated May 14, 2003.) It will be shown, hereinbelow, the invention according to claims 22-36 could not have been suggested even over the combined teachings of the newly formulated rejections. Accordingly, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

The present invention is directed to a semiconductor device in which a resin body is used for sealing the semiconductor chip, the inner lead portion of the plural leads of the package device, the die pad of the lead frame and the bonding wires, the latter electrically connecting the inner leads with the bonding pads of the chip. The invention also employs an organic film to cover the main surface of the semiconductor chip, the main surface corresponding to that having the semiconductor elements and bonding pads of the chip formed thereat (the organic film having openings for exposing the bonding pads). Such featured aspects as that just described are called for in each of independent claims 22 and 29. Both of these claims also call for the rear surface of the semiconductor chip to be fixed to the die pad by an adhesive and, moreover, for the die pad to have a size smaller than that of the chip, with respect to a plane view thereof. An example of the present invention is seen with regard to Figs. 1-3 of the present invention, although not limited thereto, which illustrate a TQFP (Thin Quad Flat Package), which is described beginning on page 10, line 24, of the present Specification.

A main featured aspect of the invention according to claims 22+ and 29+ is the use of a die pad that is smaller in size than that of the chip as well as

employing an organic film to cover the main surface of the chip, as presently set forth. In the case of using a smaller-sized die pad adhered to the rear surface of the chip (in order to reduce occurrence of a package crack in the vicinity of the back of the die pad), the present inventors, as a result of their investigative efforts, have discovered that using, also, an organic insulating film such as a polyimide film as a surface coating on the front or main surface of the chip leads to a balance in the vertical adhesion strength of the respective materials between that of the sealing resin and the chip and prevents package cracks which would otherwise result due to undesired stress concentrations. Namely, since the plan view area covered by the die pad (e.g., 5 in Fig. 2) is smaller than that of the semiconductor chip (e.g., 2), the common area covered by the rear surface of the chip and that of the die pad is relatively small while the remaining portion of the rear surface of the chip is adhered, via the adhesive (e.g., 9), with the resin material of the resin sealing body, which leads to a strong adhesion of the back surface of the chip. As a result, occurrences of package cracks in the underside of the die pad are restrained. Also, according to the present invention, as can be seen by the example embodiment of in Fig. 2 of the drawings, occurrence of the package crack in the vicinity of the main surface of the semiconductor chip is similarly restrained as a result of also providing a layer of organic material (e.g., 8 in Fig. 3) which has a high affinity (with good adhesion) with that of the resin material of the resin body (e.g., 1) as compared with that of the final passivation film (e.g., 7), which is made of inorganic material. That is, according to the present invention, good adhesion characteristics are attained with the resin of the

package at both the front and back sides of the semiconductor chip. A semiconductor device structured as that presently called for in claims 22+ and 29+ realizes an improvement in reflow crack resistance. It is submitted, such a scheme as that defined according to claims 22+ and 29+ could not have been achievable in the manner as that alleged in the above named outstanding rejections. Supportive discussion regarding this is provided hereinbelow.

Kajihara et al, it is submitted, neither disclosed nor suggested that featured aspect of the invention calling for an organic film covering the main surface of the semiconductor chip. Kajihara et al, merely disclosed a resin mold package (e.g., 30, in Fig. 30) which may have a smaller die pad (e.g., 3) than that of the chip (e.g., 2). It was an objective of Kajihara et al to increase the contact area of the rear side of the chip in the sealing resin so as to enhance the adhesion properties between that of the chip and the sealing resin as well as prevent moisture from seeping therethrough onto the chip rear surface, which would be caused by reflow cracks. However, Kajihara et al did not discuss nor make any inference regarding any relationship between the small mounting portion of the chip and that of the surface coating of the semiconductor chip and, further, made no mention of the type of materials used for coating the chips surface. Also, there is no discussion or suggestion by Kajihara et al, concerning the constitution of the several cross-hatching film layers on the front surface of the semiconductor chip 2 with regard to their Fig. 30.

Kajihara et al sought to improve the reflow cracking resistance by enlarging the adhered area between that of the rear surface of the silicon chip and the

sealing resin. This was done through making the plan view size of the die pad to which the rear surface of the chip is mounted relatively small to that of the chip rear surface. Kajihara et al, it is submitted, neither disclosed nor made reference to any relation involving the chip small mounting portion and the chip surface coating nor, for example, were concerned with the type of materials for coating the chip surface. As stated above, other than illustrating a film layer with cross-hatchings, there is no description or suggestion that such layer involves any particular type of insulating film or the like. That is, Kajihara et al neither disclosed nor suggested employing an insulating film on the chip surface in connection with achieving improved reflow cracking resistance.

Yamamoto disclosed a packaged structure of forming a photo sensitive polyimide film on the chip surface, the polyimide film being a film of organic material. However, Yamamoto also neither disclosed nor made any reference to any relation between that of a size of a chip mounting portion, on the rear surface of the chip, and the photo sensitive polyimide film on the front surface of the chip, from the viewpoint of achieving a balance in stress between the front and rear surfaces of the chip. This is obviously reinforced from the fact that the chip mounting portion according to Yamamoto is larger in size than the chip itself (see Fig. 2 thereof).

It is alleged that the techniques taught by Kajihara et al and Yamamoto are combinable. In addition to employing a photosensitive polyimide film on the main surface of the semiconductor chip, it is alleged that Yamamoto disclosed that parts of the resin body are contacting with parts (a portion) of

the rear surface of the semiconductor chip and, further, that the organic film (e.g., 4 in Fig. 1(d) in Yamamoto) provides for improved reflow cracking resistance, as argued on page 4, lines 3-7, of the outstanding Office Action. It is submitted, however, Yamamoto did not entirely teach or suggest a structure calling for parts of the resin body to be in contact with a portion of the rear surface of the semiconductor chip and that the organic film 4 of Yamamoto leads to an improved reflow cracking resistance. In order for such featured aspects to be met, the plan view area of the die pad must necessarily be smaller than that of the semiconductor chip, which is in clear contradistinction with that according to Yamamoto. That is, there is no disclosure or suggestion in Yamamoto that a part of the sealing resin contacts with a part of the rear surface of the chip as that presently set forth (in which the structure with a die pad must necessarily be smaller than that of the chip) nor any disclosure or suggestion that the organic film 4 balances stress differences and leads to an improved reflow cracking resistance.

Mori was cited for showing a resin-sealed semiconductor device. In particular, Mori disclosed a technique for forming polyimide films on <u>both</u> the front surface of the chip and on the rear surface of an island (the chip mounting portion). Mori, it is submitted, neither discussed nor made reference to any relation between the size of the chip mounting portion and the polyimide film from the viewpoint of a stress balance relationship between that of the front and rear surfaces of the chip. Accordingly, one or ordinary skill would not have been motivated to apply Mori's technique to modify that taught by Kajihara et al. Assuming, *arguendo*, one of ordinary skill would have

attempted to combine the teachings of Mori to that of Kajihara et al's technique, the forming of a polyimide film must necessarily be effected therefor on both sides of the chip, that is, on the front surface of the chip as well as on the rear surface of the island (the chip mounting portion). However, that is not what the present invention calls for. It is submitted, consideration of applying the polyimide film on the front surface of the chip to a structure as that presently called for is an idea realized by the present inventors and could only have been achieved, even from the combined teachings of Kajihara et al, Yamamoto and Mori, as a result of prior knowledge of the present invention.

Umehara disclosed a scheme in which elimination or reduction of package cracks are achieved by fixedly mounting a semiconductor chip (e.g., 10 in Fig. 1) to a relatively smaller-sized die pad (e.g., 81) using adhesive (e.g., 84), the adhesive containing thermo-plastic polyimide as a major component thereof. Although Umehara et al taught a scheme in which the plan view covered by the die pad is smaller than that of the semiconductor chip, Umehara, as admitted in the Office Action, "*fail[ed] to explicitly show an organic film formed to cover said main surface ...* ."

The second rejection, beginning on the bottom of page 4 of the outstanding Office Action similarly combines the teachings of Mori with that of Umehara et al for the same and similar reasons as that combining Mori's teachings with that of Kajihara et al and Yamamoto. With regard to this rejection, similarly, there is neither a reason given nor any motivation for applying Mori's technique to that of Umehara et al. In fact, even if one of ordinary skill, *arguendo*, would have attempted to apply Mori's teachings to

Umehara et al's resin package device, the invention still would not have been realizable. This is because if Mori's teachings were to have been applied to that of Umehara et al, the polyimide films must necessarily be provided on both the front as well as on the rear surfaces of the island (chip mounting portion), which is in clear contradistinction with that presently called for. For at least these reasons, the invention could not have been achievable, even also over the combined teachings of Umehara et al and Mori.

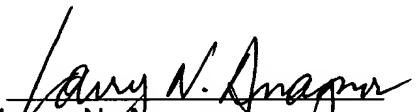
The additional comments hereinbelow address the added discussion on page 6 of the Office Action. It is alleged on page 6, lines 4-7, of the outstanding Office Action, that claimed subject matter directed to the combination of the organic film and the small die pad are only individually detailed with regard to separate drawing figures. However, a careful review of the Specification and drawing illustration shows that they are, in fact, covered by the same embodiment. In fact, as can be seen from page 10, line 24, to page 11, line 3, as well as the detailed description directed thereto, beginning on page 11, line 4 thereof, Figs. 1, 2 and 3 relate to the same disclosed embodiment of a TQFP (Thin Quad Flat Package), directed to one example embodiment of the present invention. For example, it is noted that Fig. 3 is an enlarged sectional view of only the semiconductor chip 2 in Fig. 2 of the drawings. Therefore, it is apparent (from the context of those two illustrations and the related description, beginning on page 11) that the sectional view in Fig. 3 pertains solely to the semiconductor chip and not a cross-section of the resin sealed package itself. It is submitted, the Specification in conjunction

with the related drawing illustrations must be considered in their entirety when relating the same to the claimed subject matter.

Therefore, in view of the above supportive discussion/rebuttal arguments regarding the outstanding art rejections, reconsideration as well as favorable action on all of the presently pending claims, i.e., claims 22-36, and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (843.37610X00).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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